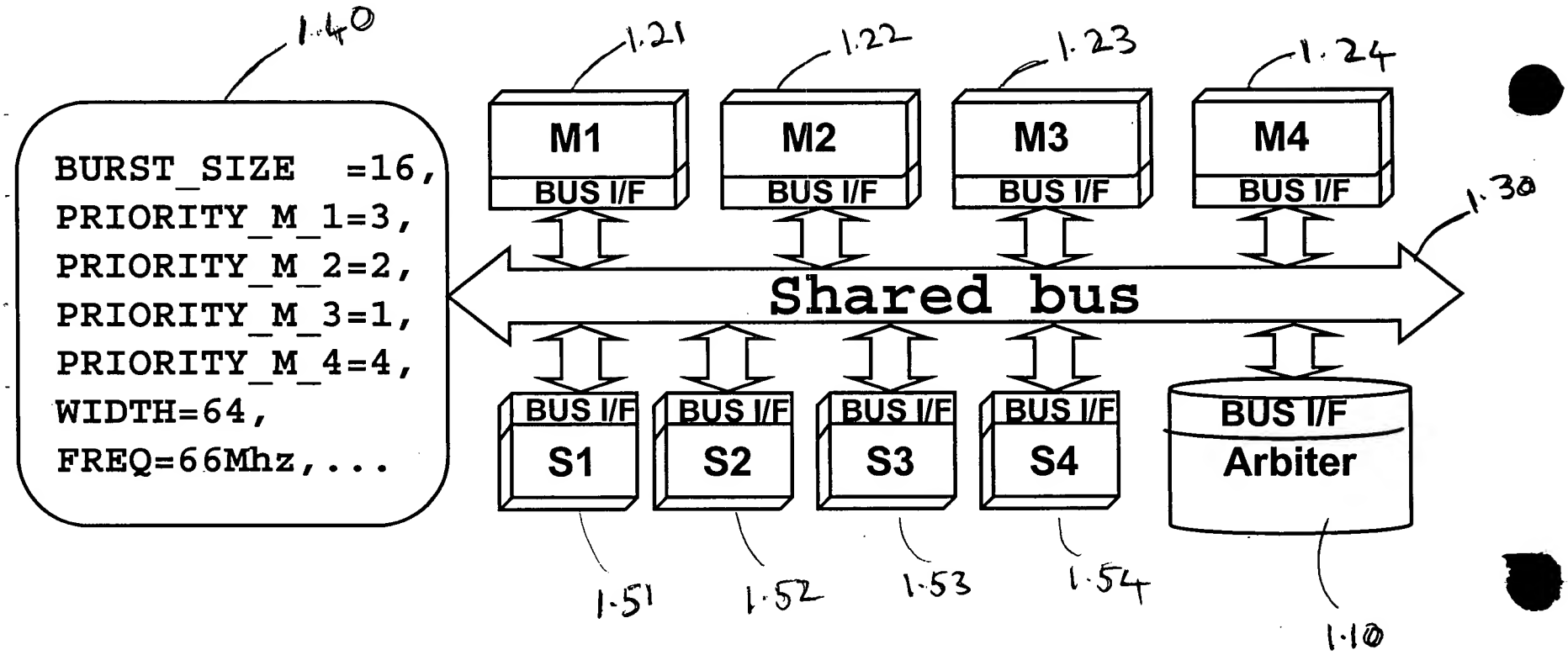
1.40
BURST_SIZE =16,
PRIORITY_M_1=3,
PRIORITY_M_2=2,
PRIORITY_M_3=1,
PRIORITY_M_4=4,
WIDTH=64,
FREQ=66Mhz,...
1.21
1.22
1.23
1.24
M1
M2
M3
M4
BUS I/F
BUS I/F
BUS I/F
BUS I/F
1.30
Shared bus
BUS I/F
BUS I/F
BUS I/F
BUS I/F
BUS I/F
S1
S2
S3
S4
Arbiter
1.51
1.52
1.53
1.54
1.10

FIG.1

T09090 E2Eh2860

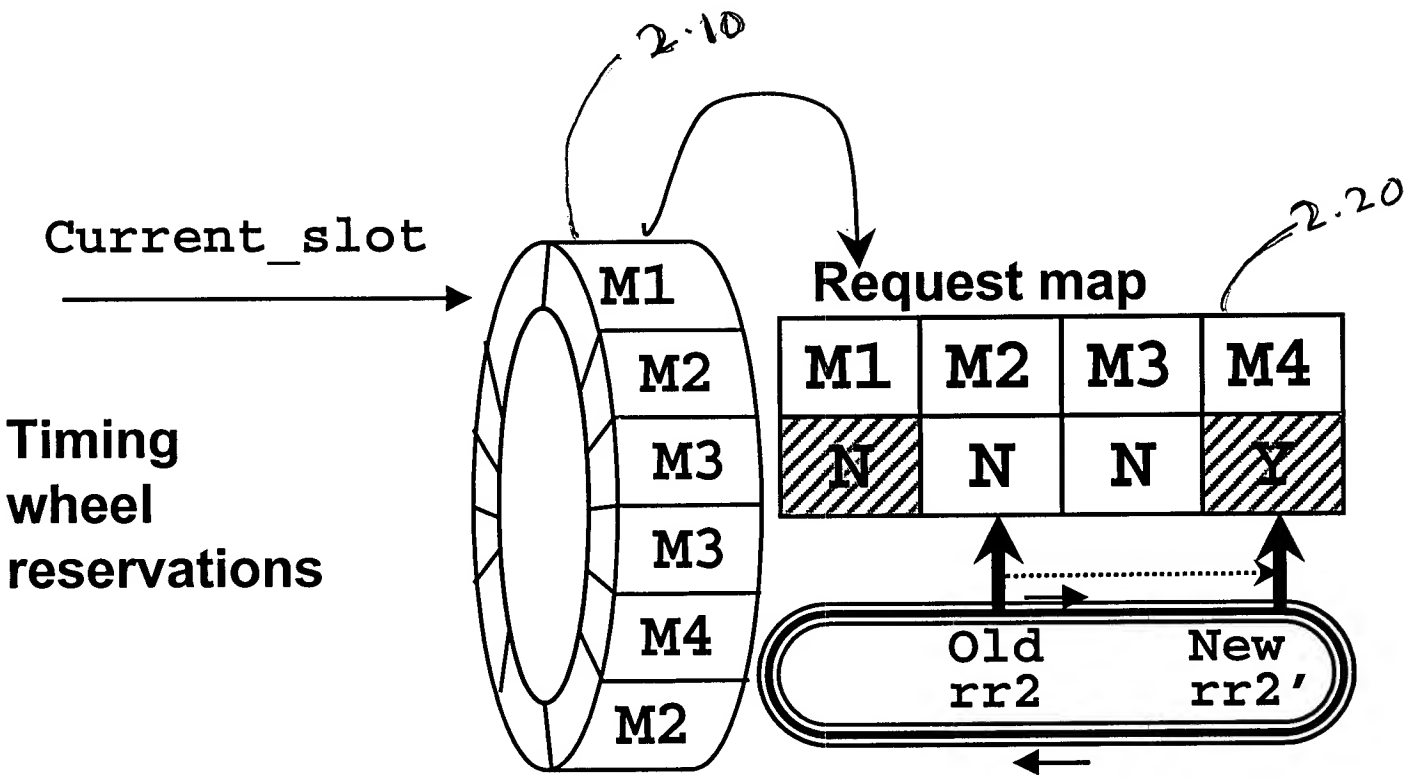


FIG.2(a)

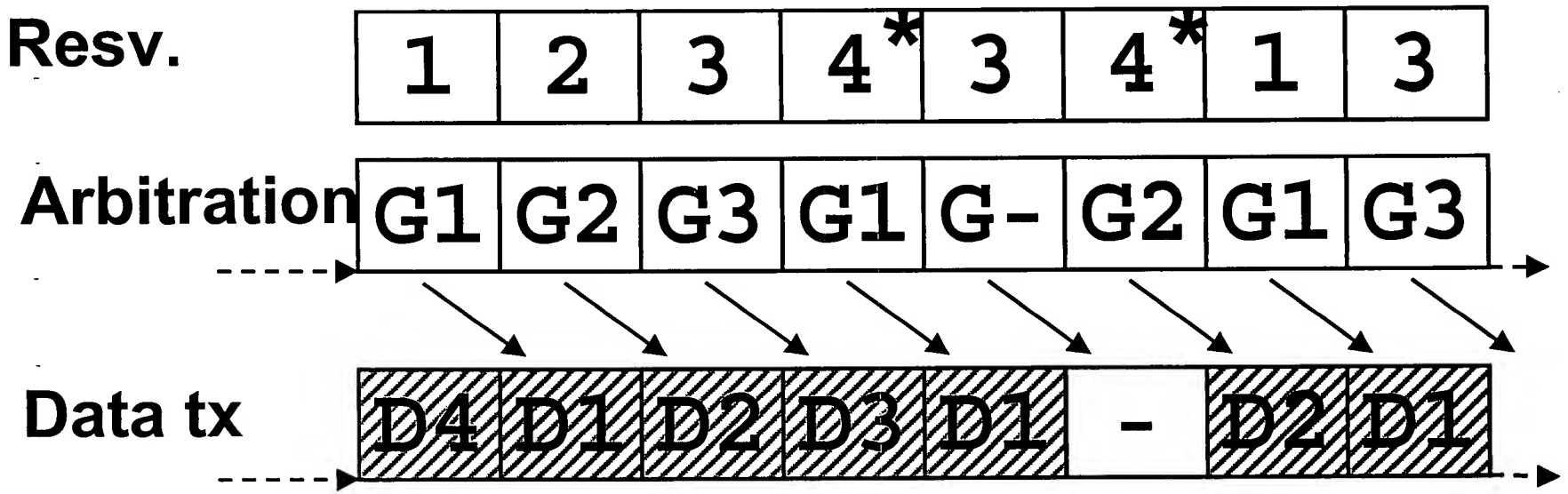
Resv.
1
2
3
4*
3
4*
1
3
Arbitration
G1
G2
G3
G1
G-
G2
G1
G3
Data tx
D4
D1
D2
D3
D1
-
D2
D1

FIG.2(b)

TOSO90 E2Enz86D

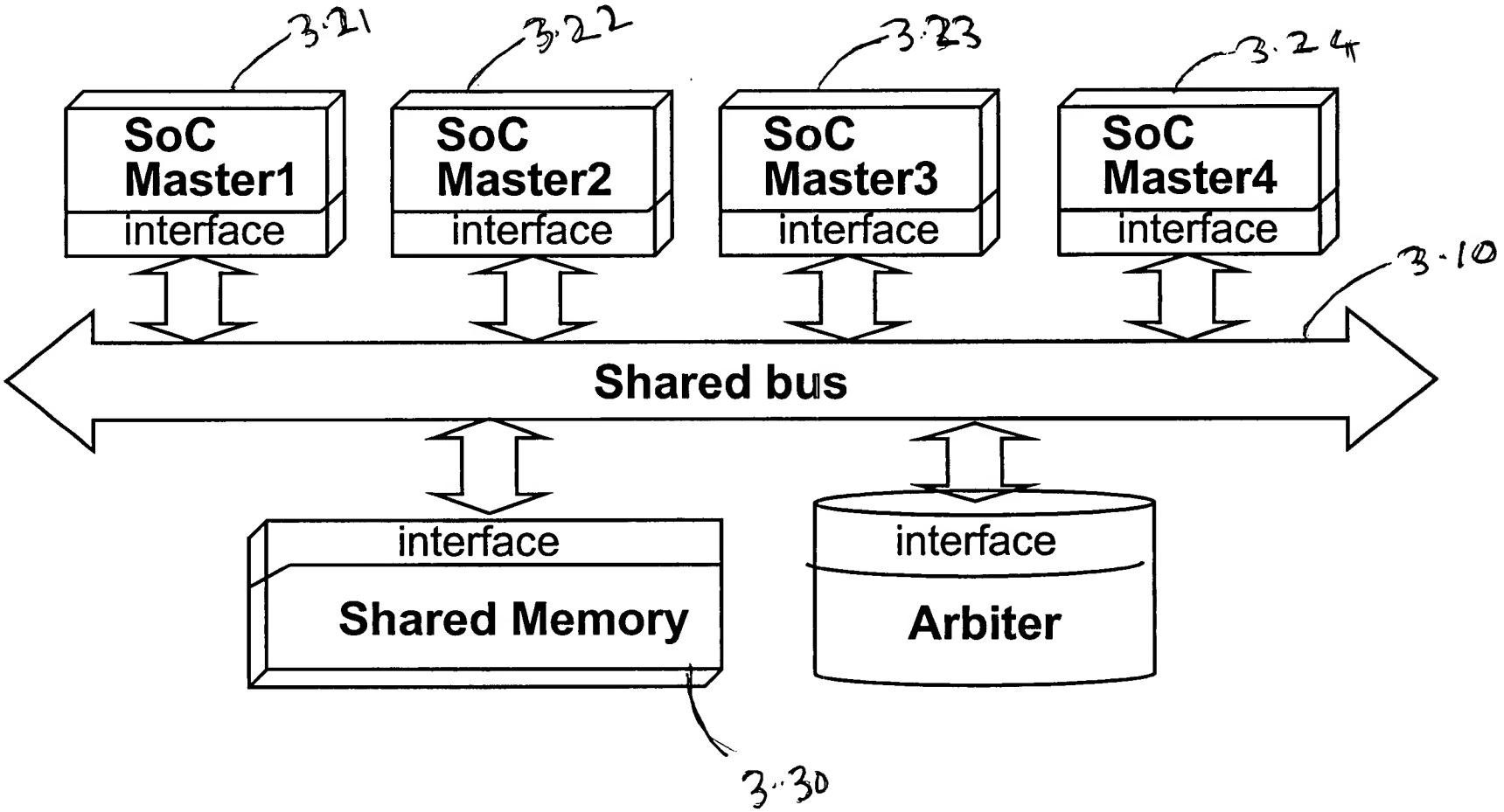


FIG.3(a)

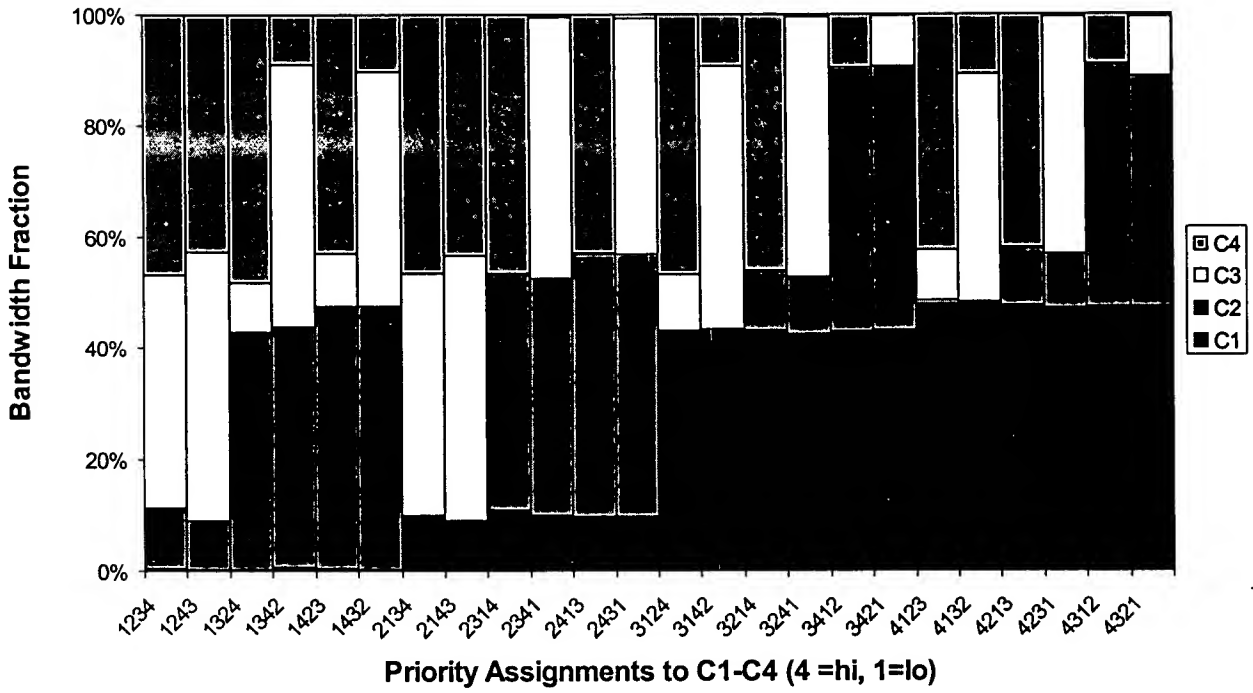
100%
80%
60%
40%
20%
0%
Bandwidth Fraction
C4
C3
C2
C1
1234
1243
1324
1342
1423
1432
2134
2143
2314
2341
2413
2431
3124
3142
3214
3241
3412
3421
4123
4132
4213
4231
4312
4321
Priority Assignments to C1-C4 (4 =hi, 1=lo)

FIG.3(b)

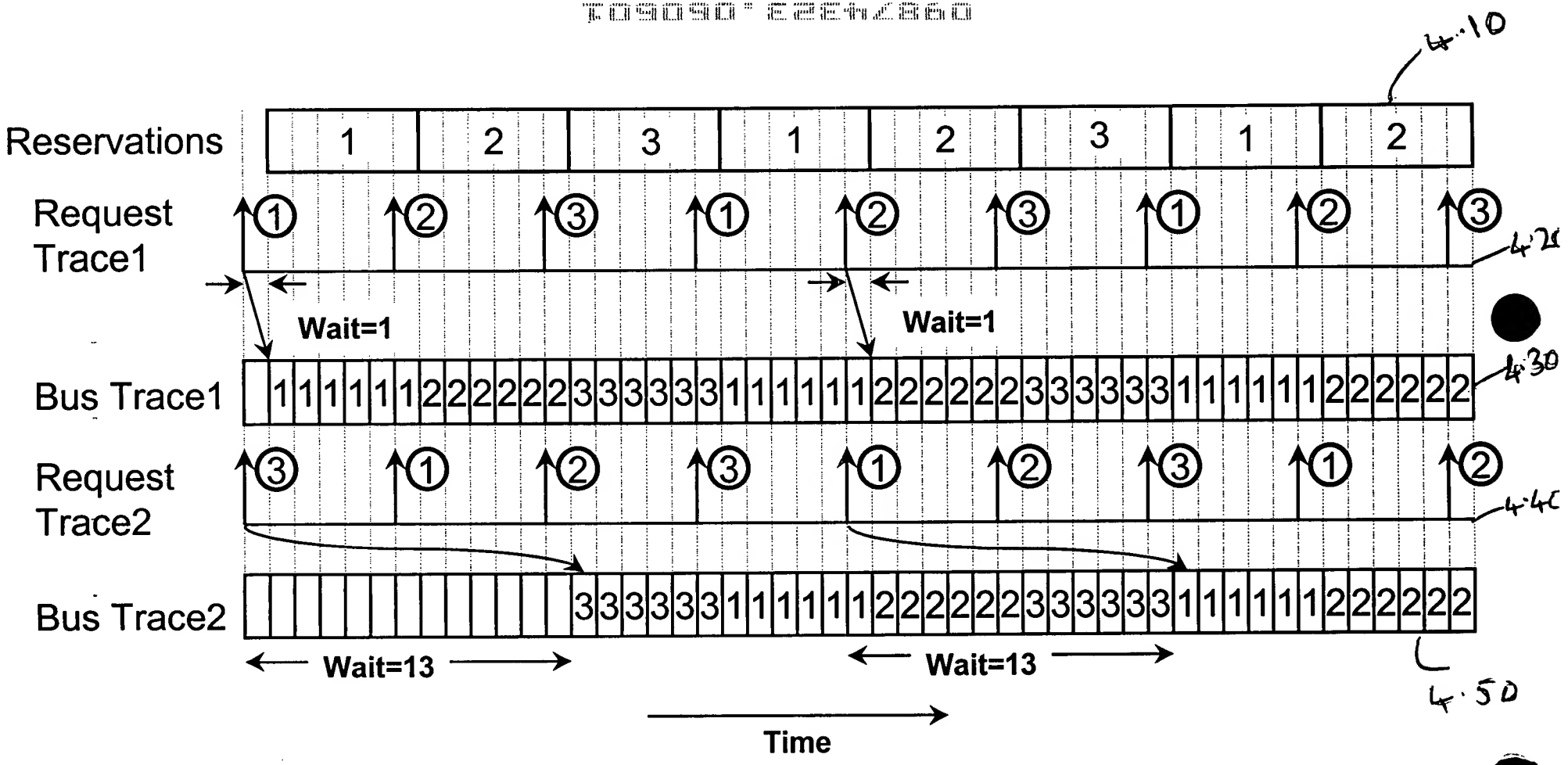
Reservations
1
2
3
1
2
3
1
2
Request Trace1
Wait=1
Wait=1
Bus Trace1
Request Trace2
Bus Trace2
Wait=13
Wait=13
Time

FIG.4

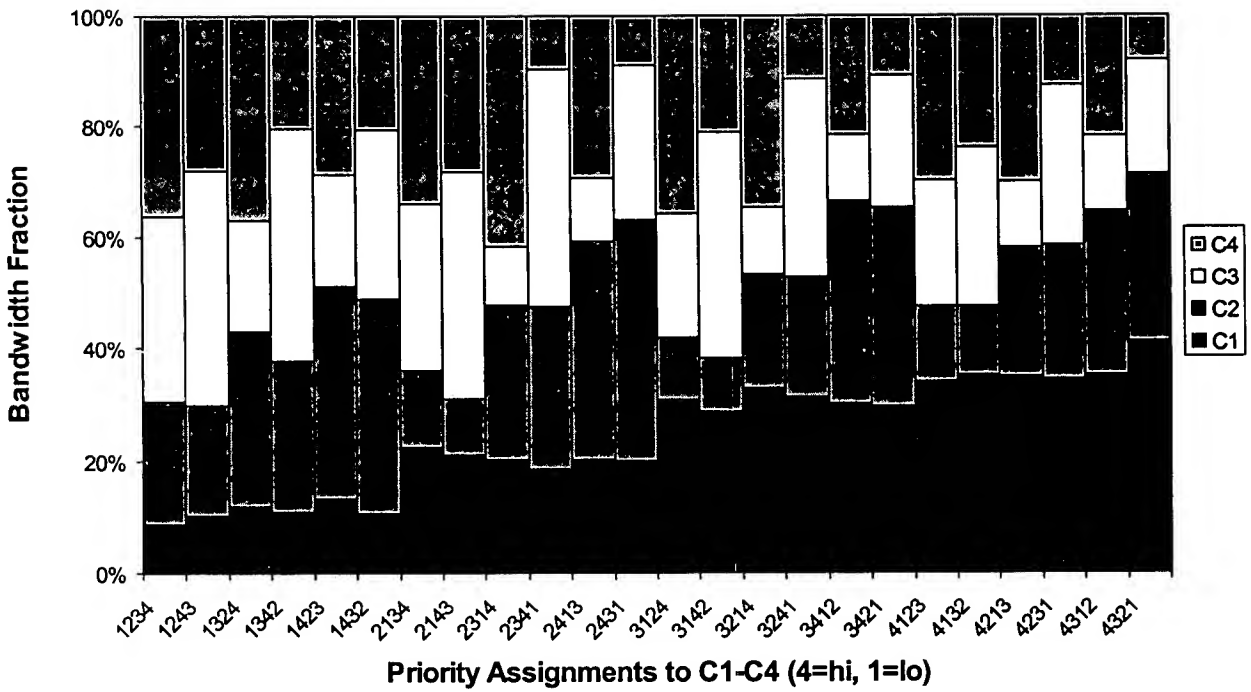
100%
80%
60%
40%
20%
0%
Bandwidth Fraction
C4
C3
C2
C1
1234
1243
1324
1342
1423
1432
2134
2143
2314
2341
2413
2431
3124
3142
3214
3241
3412
3421
4123
4132
4213
4231
4312
4321
Priority Assignments to C1-C4 (4=hi, 1=lo)

FIG.5

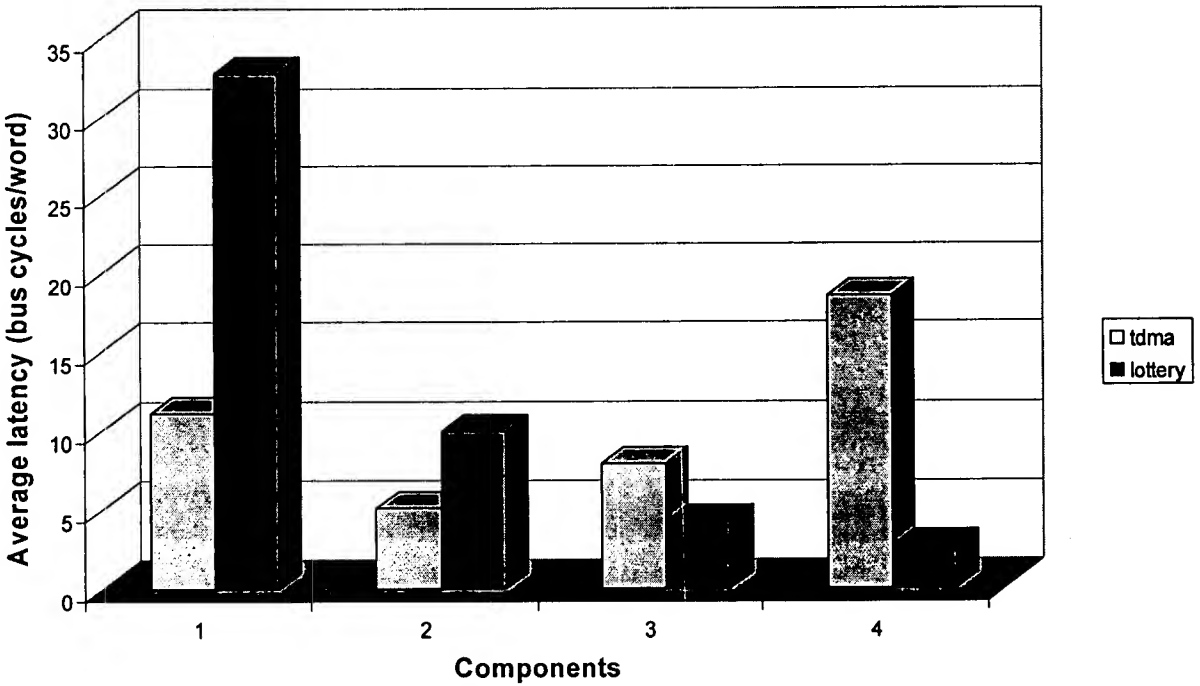
Average latency (bus cycles/word)
35
30
25
20
15
10
5
0
1
2
3
4
Components
tdma
lottery

FIG.6

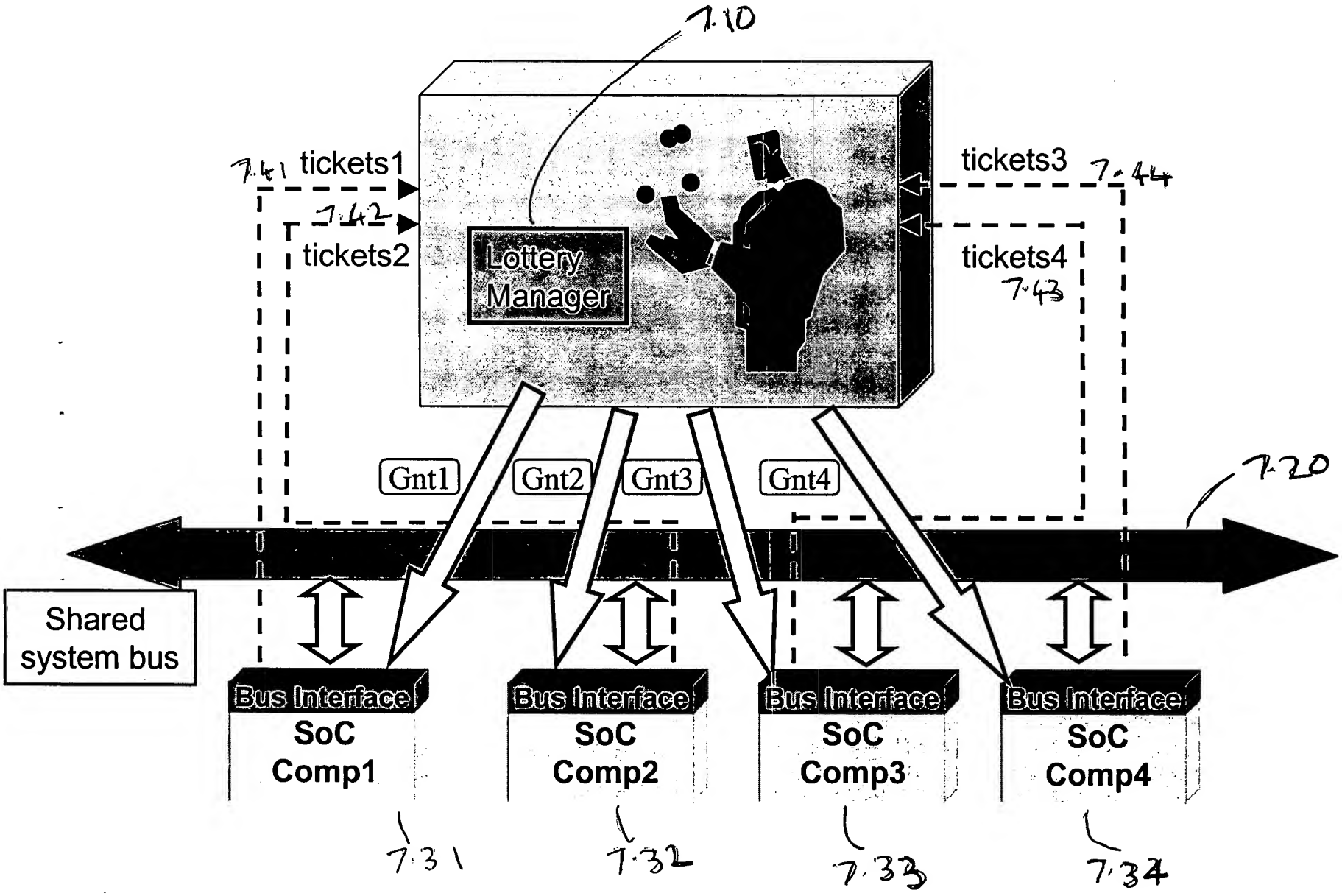
7.10
7.41
tickets1
7.42
tickets2
Lottery Manager
tickets3
7.44
tickets4
7.43
Gnt1
Gnt2
Gnt3
Gnt4
7.20
Shared system bus
Bus Interface
SoC Comp1
Bus Interface
SoC Comp2
Bus Interface
SoC Comp3
Bus Interface
SoC Comp4
7.31
7.32
7.33
7.34

FIG.7

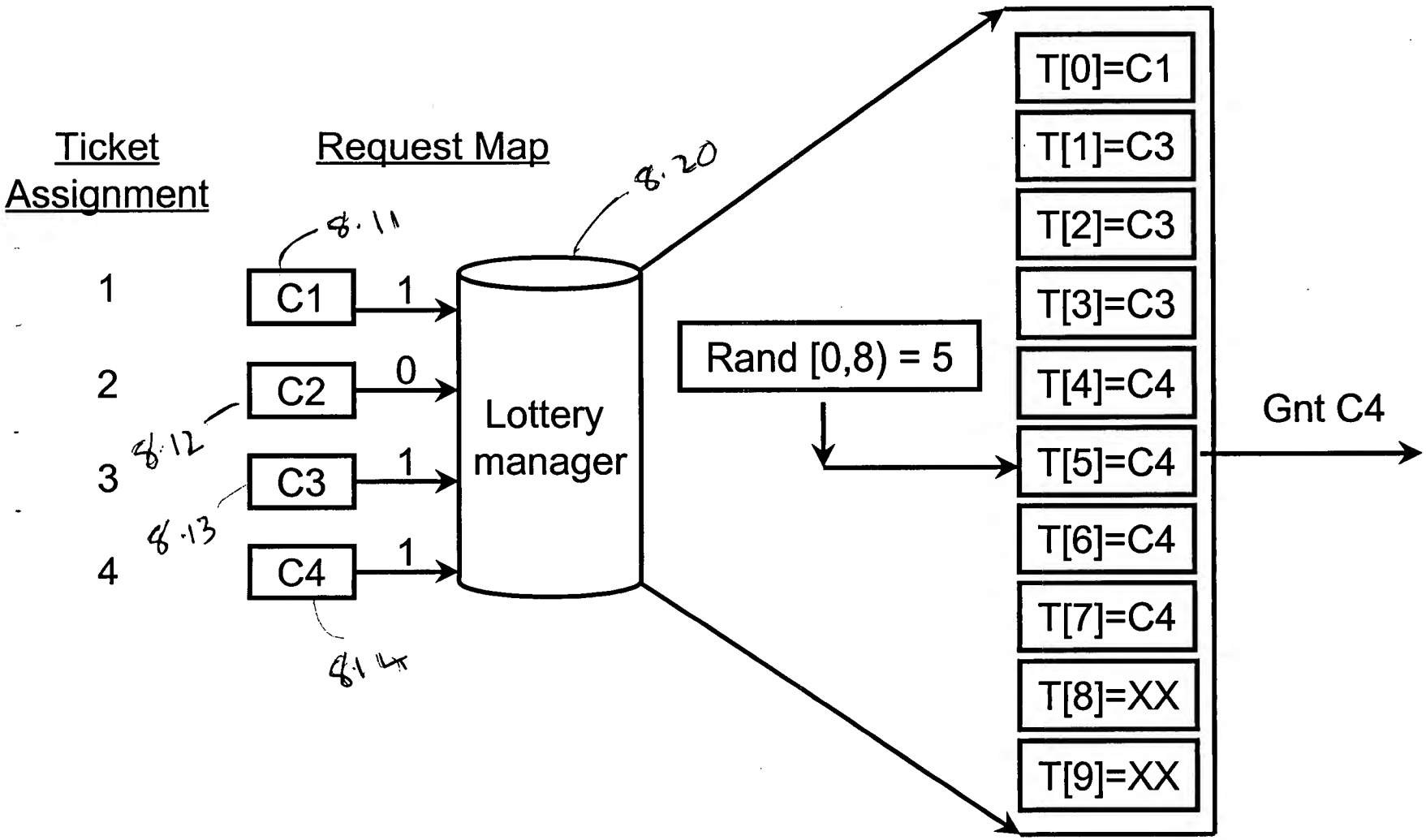
Ticket Assignment
Request Map
8.11
8.20
1
2
3
4
C1
C2
C3
C4
1
0
1
1
8.12
8.13
8.14
Lottery manager
Rand [0,8) = 5
T[0]=C1
T[1]=C3
T[2]=C3
T[3]=C3
T[4]=C4
T[5]=C4
T[6]=C4
T[7]=C4
T[8]=XX
T[9]=XX
Gnt C4

FIG.8

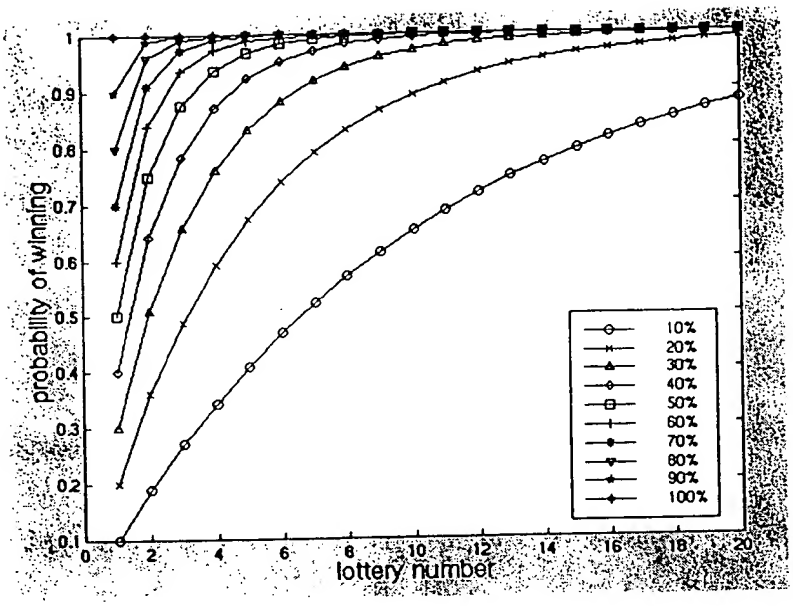
probability of winning
lottery number
10%
20%
30%
40%
50%
60%
70%
80%
90%
100%

FIG. 9

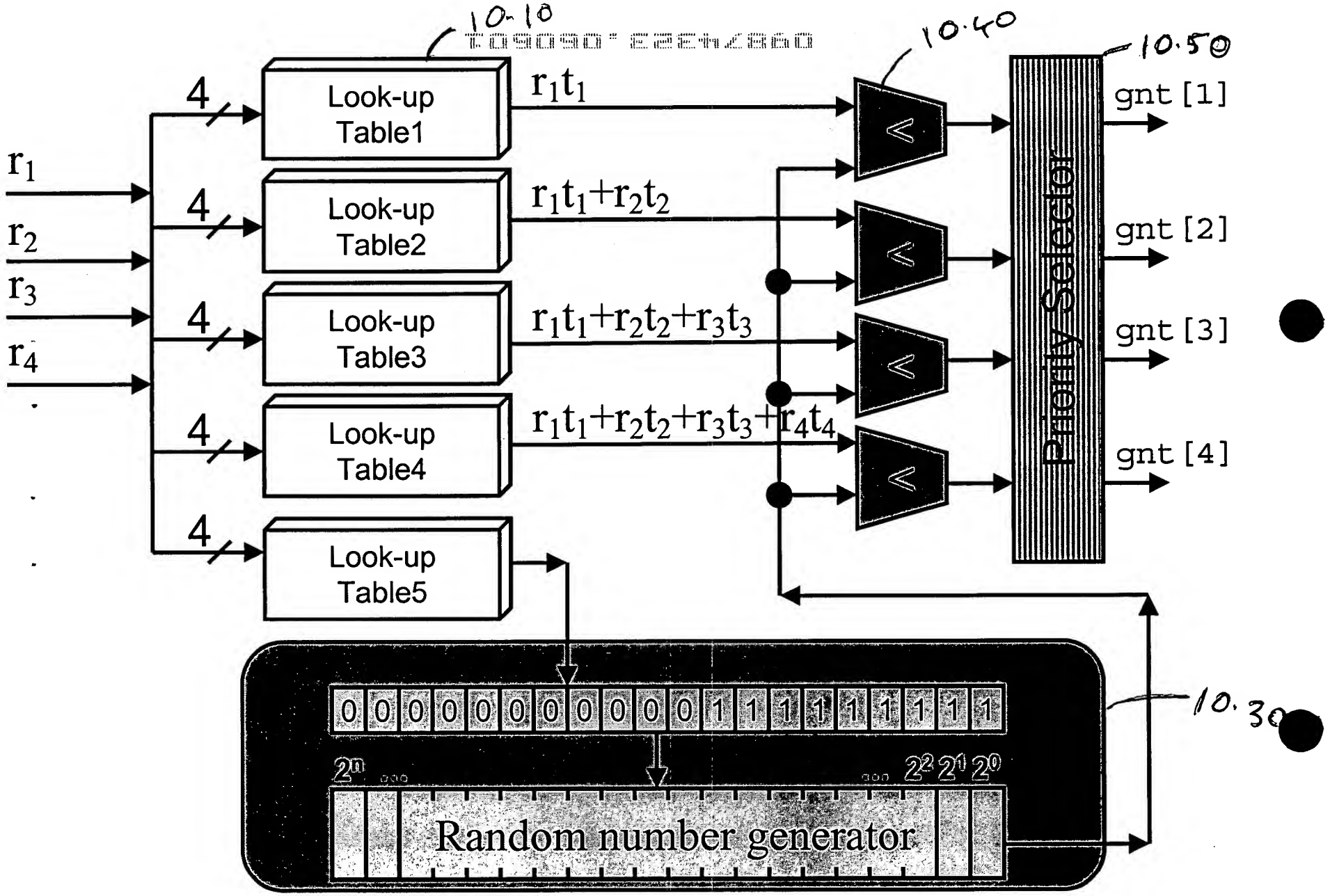
10.10
10.40
10.50
10.30
4
Look-up Table1
Look-up Table2
Look-up Table3
Look-up Table4
Look-up Table5
$r_1$
$r_2$
$r_3$
$r_4$
$r_1t_1$
$r_1t_1+r_2t_2$
$r_1t_1+r_2t_2+r_3t_3$
$r_1t_1+r_2t_2+r_3t_3+r_4t_4$
<
Priority selector
gnt [1]
gnt [2]
gnt [3]
gnt [4]
0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
$2^n$
$2^2$ $2^1$ $2^0$
Random number generator

FIG.10

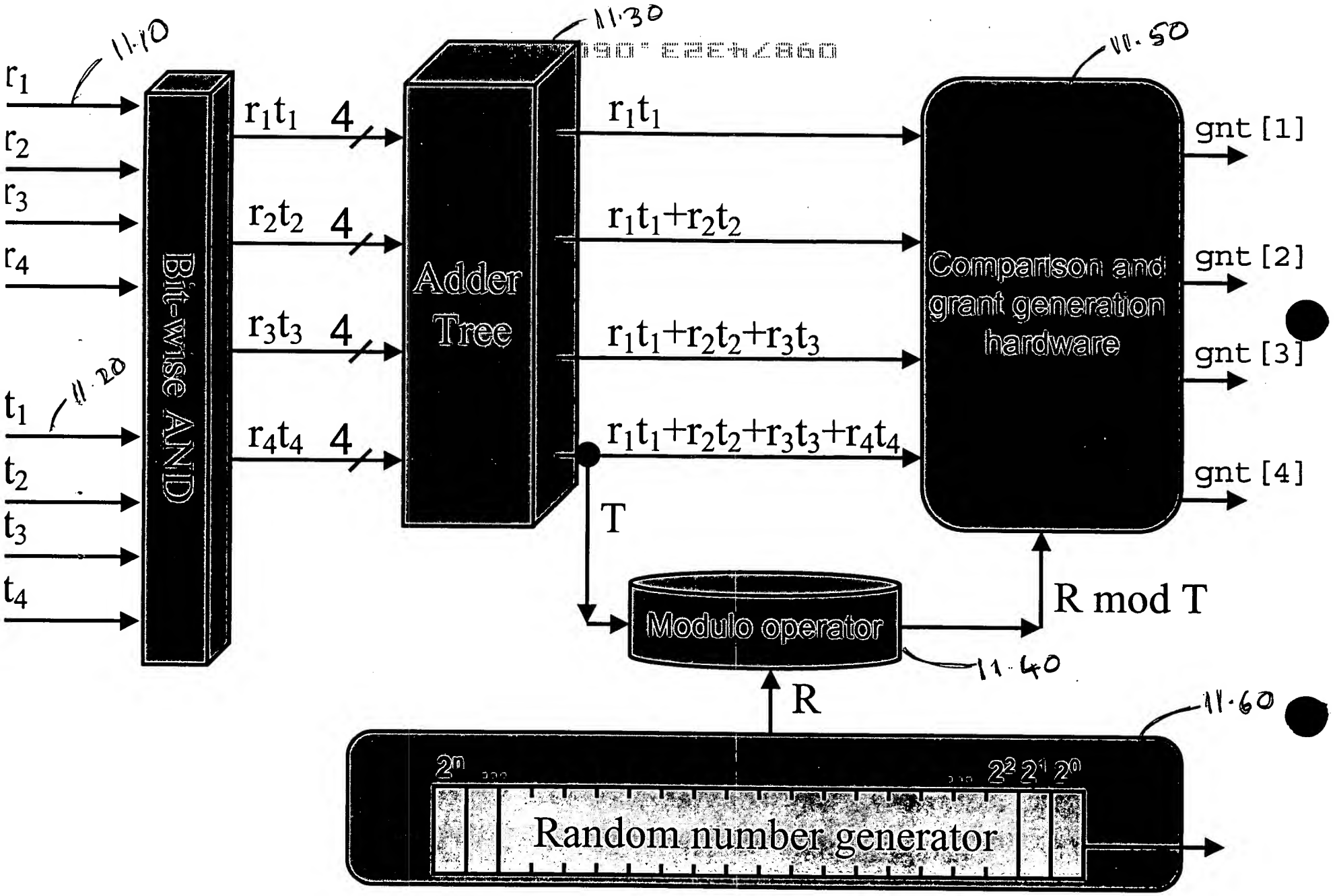
11.10
11.30
11.50
11.20
11.40
11.60
r1
r2
r3
r4
t1
t2
t3
t4
Bit-wise AND
r1t1 4
r2t2 4
r3t3 4
r4t4 4
Adder Tree
r1t1
r1t1+r2t2
r1t1+r2t2+r3t3
r1t1+r2t2+r3t3+r4t4
T
Comparison and grant generation hardware
gnt [1]
gnt [2]
gnt [3]
gnt [4]
R mod T
Modulo operator
R
2n
2² 2¹ 2⁰
Random number generator

FIG.11

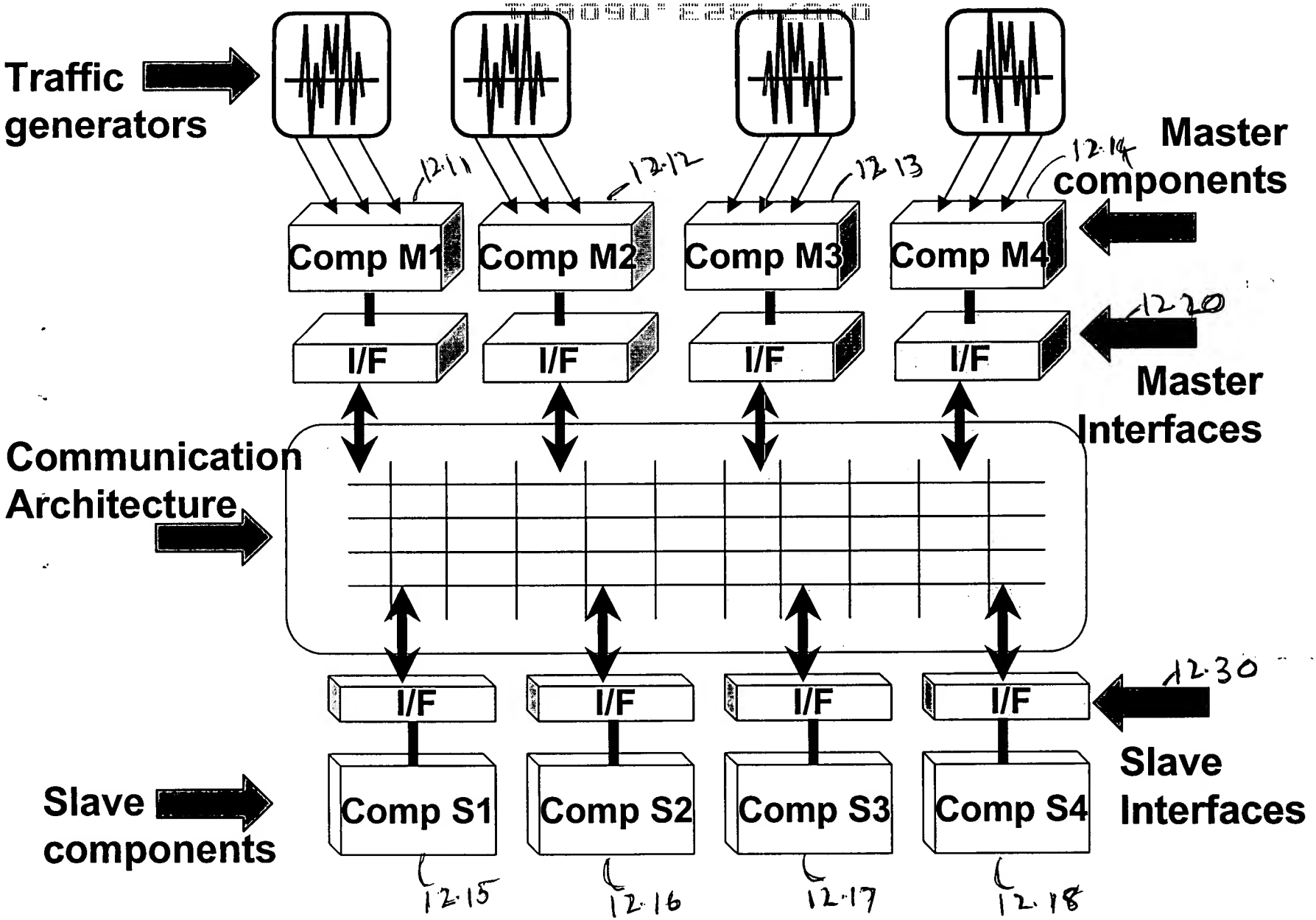
Traffic generators
Master components
Comp M1
Comp M2
Comp M3
Comp M4
1211
1212
1213
1214
I/F
1220
Master Interfaces
Communication Architecture
1230
Slave components
Comp S1
Comp S2
Comp S3
Comp S4
Slave Interfaces
1215
1216
1217
1218

FIG.12

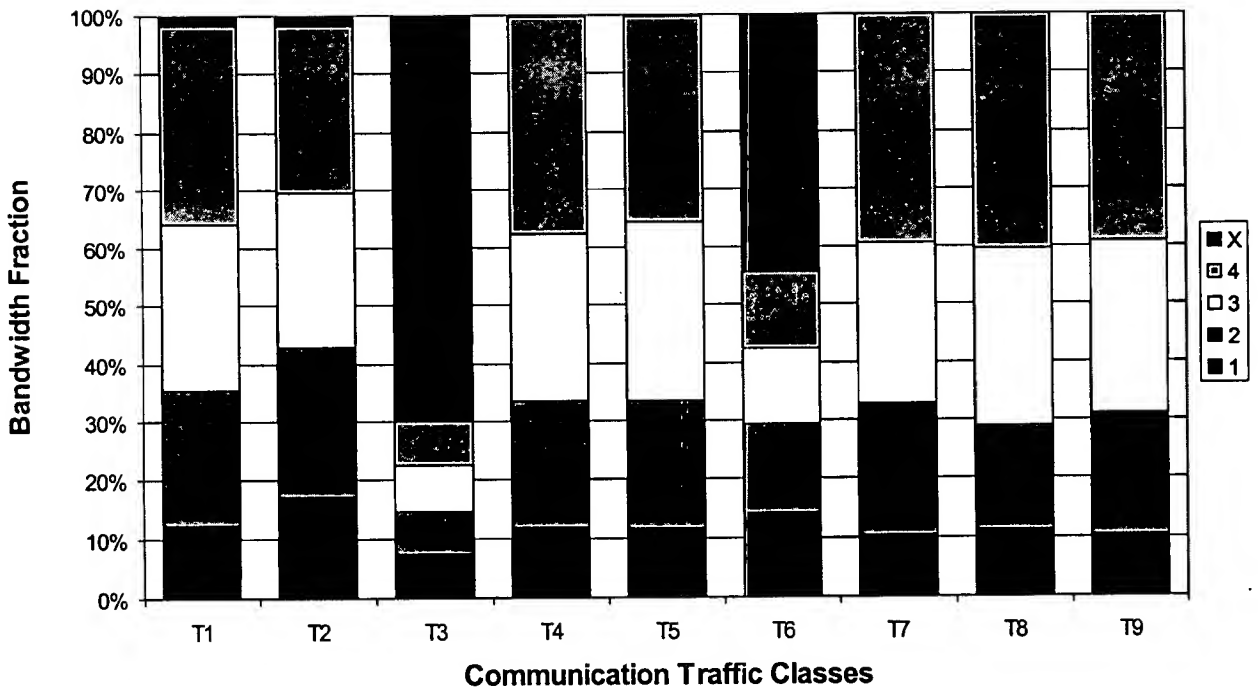
100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%
Bandwidth Fraction
T1
T2
T3
T4
T5
T6
T7
T8
T9
Communication Traffic Classes
X
4
3
2
1

FIG.13

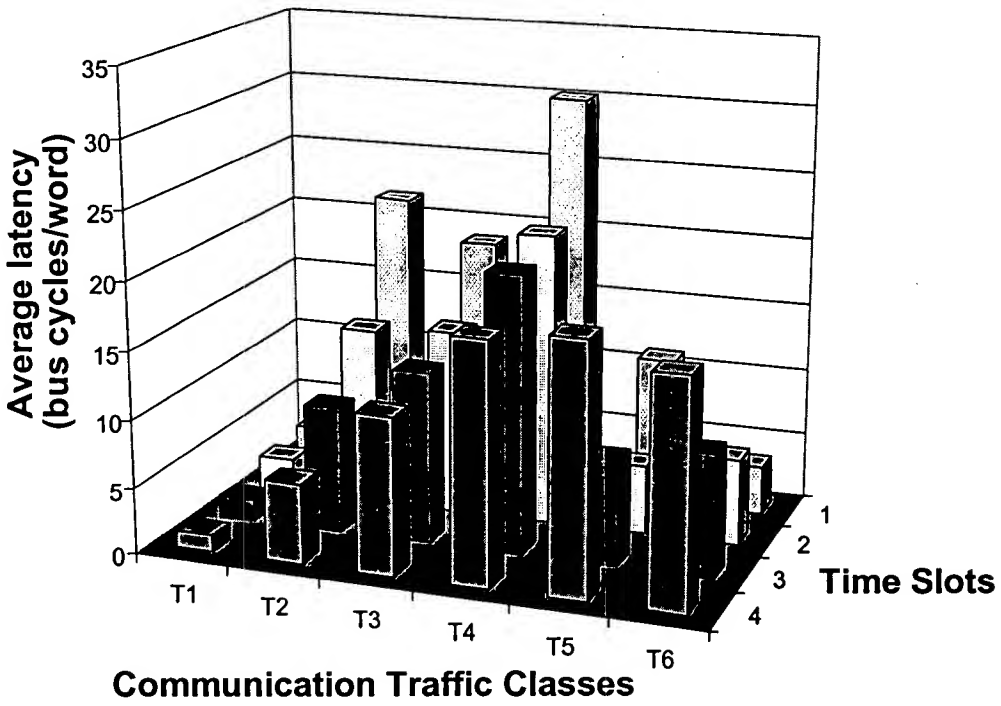
Average latency
(bus cycles/word)
35
30
25
20
15
10
5
0
T1
T2
T3
T4
T5
T6
Communication Traffic Classes
1
2
3
4
Time Slots

FIG.14(a)

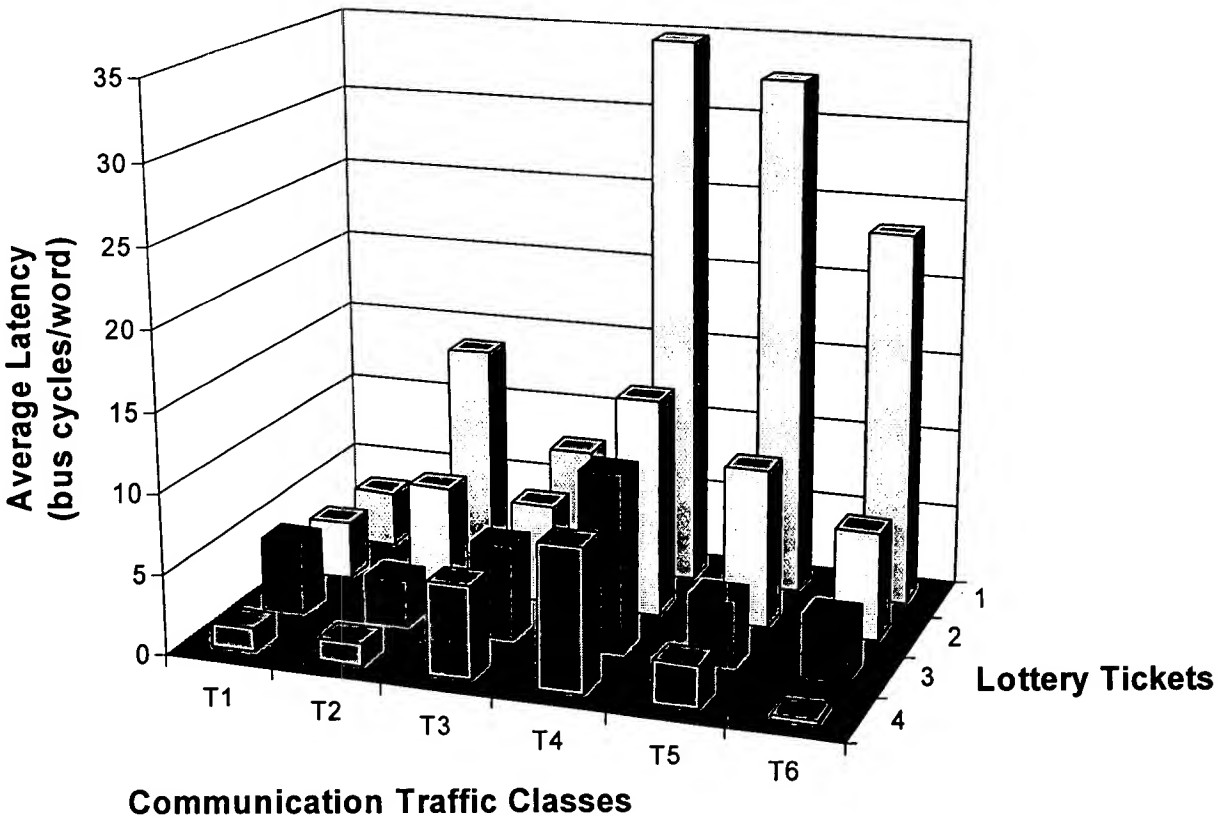
Average Latency
(bus cycles/word)
35
30
25
20
15
10
5
0
T1
T2
T3
T4
T5
T6
Communication Traffic Classes
1
2
3
4
Lottery Tickets

FIG.14(b)

TO9090 "E2E4C860

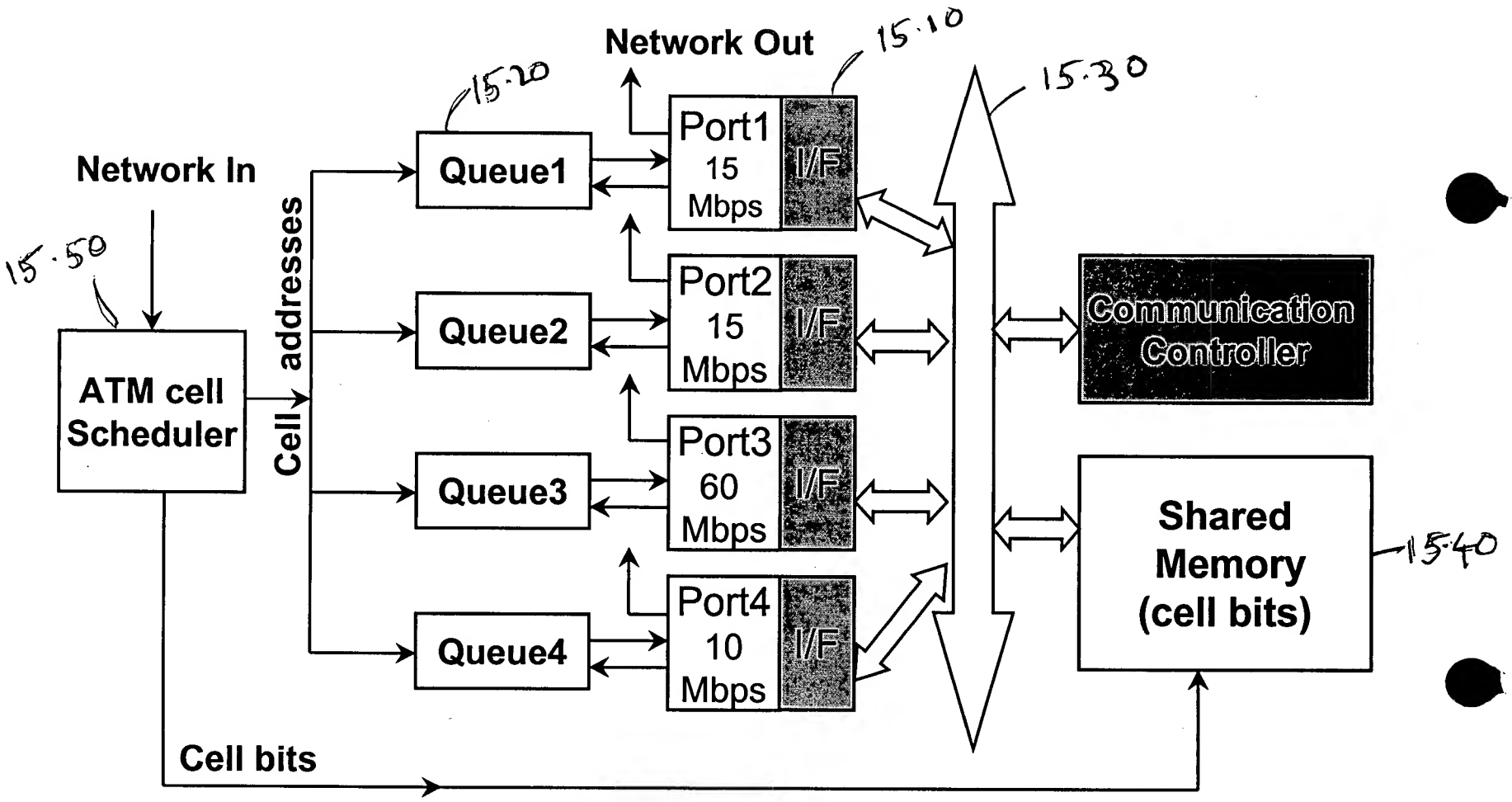


FIG.15